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06EC56

Fifth Semester B.E. Degree Examination, June/July 2013
Fundamental of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: *1. Answer FIVE full questions, selecting at least TWO questions from each part.*
2. Missing data may be assumed suitably.

PART – A

1 a. Explain briefly the nMOS enhancement mode transistor action with neat sketches. **(06 Marks)**

b. With the help of cross-sectional schematic, explain the various steps involved in n-well CMOS fabrication process. **(08 Marks)**

c. Define noise margin. Calculate the noise margins for the transfer characteristic of typical inverter, shown in Fig.Q.1(c). **(06 Marks)**

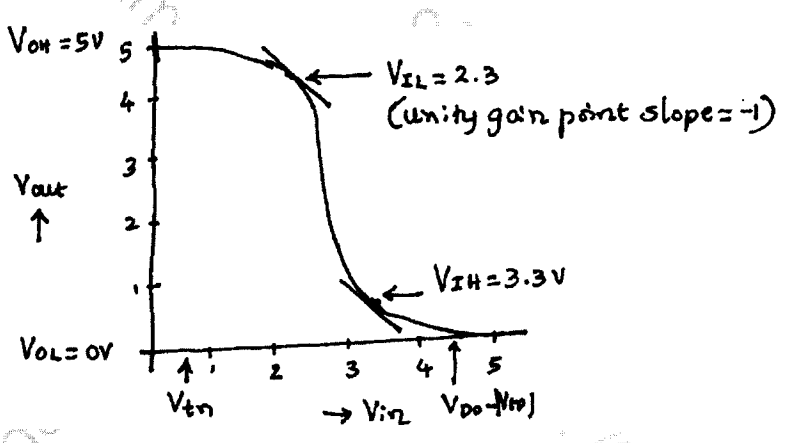

Fig.Q.1(c)

2 a. Explain briefly the circuit operation of a basic differential inverter and a Tristate inverter. **(06 Marks)**

b. Draw the circuit diagram, mono chrome stick diagram and mask layout of p-well CMOS inverter. **(08 Marks)**

c. Distinguish burried and butting contacts with suitable diagrams. **(06 Marks)**

3 a. Draw the circuit diagram and monochrome stick diagram for two input CMOS NOR gate. **(06 Marks)**

b. What do you mean by pre-charge and evaluate modes in CMOS dynamic logic? Explain. **(06 Marks)**

c. What are single rail and dual rail networks? Explain how cascade voltage switch logic (CVSL) may be used to obtain dual-rail logic gates. **(08 Marks)**

4 a. Calculate the area capacitance values associated with the following structure, having different layers as shown in Fig.Q.4(a) (relative 'C' value for polysilicon-to-substrate = 0.1 pf × $10^{-4}/\mu m^2$ and metal 1-to-substrate = 0.075 pf × $10^{-4}/\mu m^2$). **(06 Marks)**

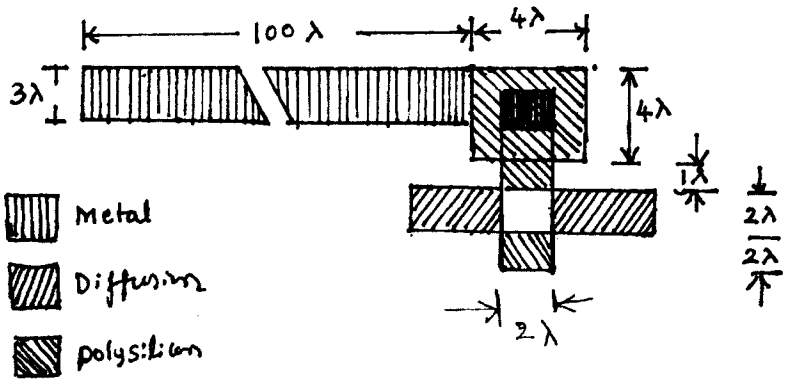

Fig.Q.4(a)

b. Prove how the delay associated with CMOS inverter pair is independent of input transitions. **(06 Marks)**

c. Write the scale factors for the following parameters:
   i) Gate capacitance (C_g)
   ii) Maximum operating frequency (f_o)
   iii) Current density (J)
   iv) Power speed product (P_T). **(08 Marks)**

PART – B

5 a. Discuss the architectural issues in the design of VLSI sub system. **(06 Marks)**
   b. Implement a 4-way multiplexer using nMOS switches. **(06 Marks)**
   c. Explain structured design approach for a parity generator. **(08 Marks)**

6 a. Realize a 4 × 4 barrel shifter using MOS switches and explain in brief its salient features. **(06 Marks)**
   b. Explain the various steps involved in designing a 4-bit adder. **(08 Marks)**
   c. Discuss on a serial-parallel multiplier approach used in adder. **(06 Marks)**

7 a. What are the system timing considerations? Explain. **(06 Marks)**
   b. Explain the circuit operation of a three-transistor dynamic RAM cell. **(07 Marks)**
   c. Show the functioning of a pseudo-static memory cell. **(07 Marks)**

8 Write short notes on the following:
   a. Input output pads.
   b. Controllability and observability.
   c. Boundary scan test (BST).
   d. Built-in-self-test (BIST). **(20 Marks)**

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